

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Yoshitaka Tsunashima et al.

U.S. Serial No. : Not Known Yet

Filing Date : March 9, 2001

For : **SEMICONDUCTOR DEVICE HAVING A GATE
INSULATING FILM STRUCTURE INCLUDING AN
INSULATING FILM CONTAINING METAL, SILICON
AND OXYGEN AND MANUFACTURING METHOD
THEREOF**

Group Art Unit : Not Yet Known

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I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" Service under 37 CFR 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington, DC 20231.

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Charles Jackson

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INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The Examiner's attention is respectfully invited to review the following enclosed and listed documents which are also listed on the accompanying Form PTO-1449, enclosed in duplicate.

U.S. PATENTS

- gmb 1. U.S. Patent No. 5,963,810, Issued: October 5, 1999 to Gardner et al., and
gmb 2. U.S. Patent No. 5,834,353, Issued: November 10, 1998 to Wu.

FOREIGN PATENTS

- gmb 1. Japanese Patent No. 11-135774, Issued: May 21, 1999 to Anthony et al., and
gmb 2. Japanese Patent No. 3-74878, Issued: May 29, 1991 to Shinriki et al.

OTHER REFERENCES

- gmb 1. Copel et al., *Structure and Stability of Ultrathin Zirconium Oxide Layers on Si(001)*, Applied Physics Letters, Vol. 76, No. 4 (1/24/00), pp. 436-438,
gmb 2. Guo et al., *High Quality Ultra-thin (1.5 nm) TiO₂Si₃N₄ Gate Dielectric for Deep Sub-micron CMOS Technology*, International Electron Device Meeting, 1999, Technical Digest, Session 6: Process Technology-High K Gate Dielectrics (December 8, 1999),
gmb 3. Lee et al., *Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application*, International Electron Device Meeting, 1999, Technical Digest, Session 6: Process Technology-High K Gate Dielectrics (December 8, 1999),
gmb 4. Luan et al., *High Quality Ta₂O₅ Gate Dielectrics with $T_{ox,eq} < 10\text{\AA}$* , International Electron Device Meeting, 1999, Technical Digest, Session 6: Process Technology-High K Gate Dielectrics (December 8, 1999),
gmb 5. Ma et al., *Zirconium Oxide Based Gate Dielectrics with Equivalent Oxide Thickness of Less Than 1.0 nm and Performance of Submicron MOSFET using a Nitride Gate Replacement Process*, International Electron Device Meeting, 1999,

Technical Digest, Session 6: Process Technology-High K Gate Dielectrics

(December 8, 1999), and

6. *QMD*

Qi et al., *MOSCAP and MOSFET Characteristics Using ZrO₂ Gate Dielectric*

Deposited Directly on Si, International Electron Device Meeting, 1999, Technical

Digest, Session 6: Process Technology-High K Gate Dielectrics (December 8, 1999).

Pursuant to Rule 37 C.F.R. §1.97(b)(3), an Information Disclosure Statement

shall be considered by the Patent Office filed before the mailing date of a first Office Action on the merits.

This Information Disclosure Statement is not a representation that the documents cited herein are considered most pertinent, or that a search has been undertaken, or that any of the cited documents are indeed prior art. The Examiner is invited to undertake an independent search. Applicants assert that the claimed invention is patentable over these documents.

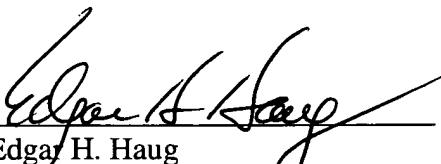
Applicants respectfully request that the Examiner consider and make of record the documents cited herein and that a copy of Form PTO-1449, appropriately initialed by the Examiner, be returned to Applicants' attorney.

It is believed no fee is due, however, the Examiner is authorized to charge any deficit or credit any overpayment to Deposit Account No. 50-0320.

Respectfully submitted,

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